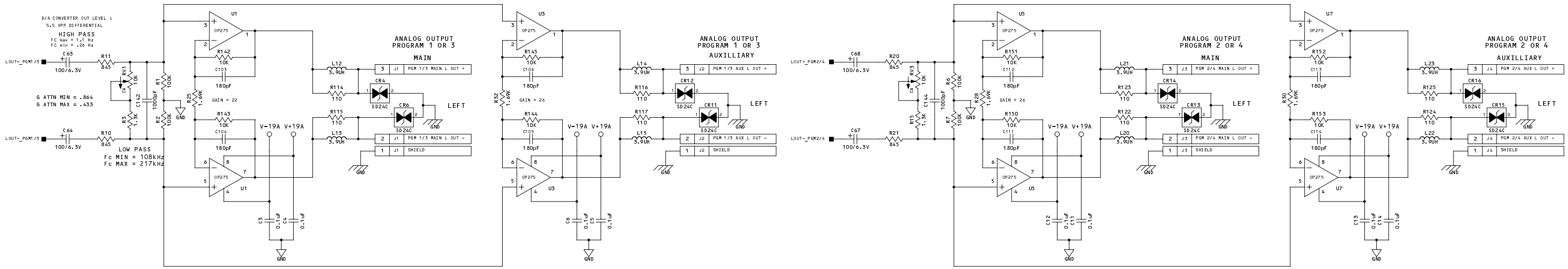
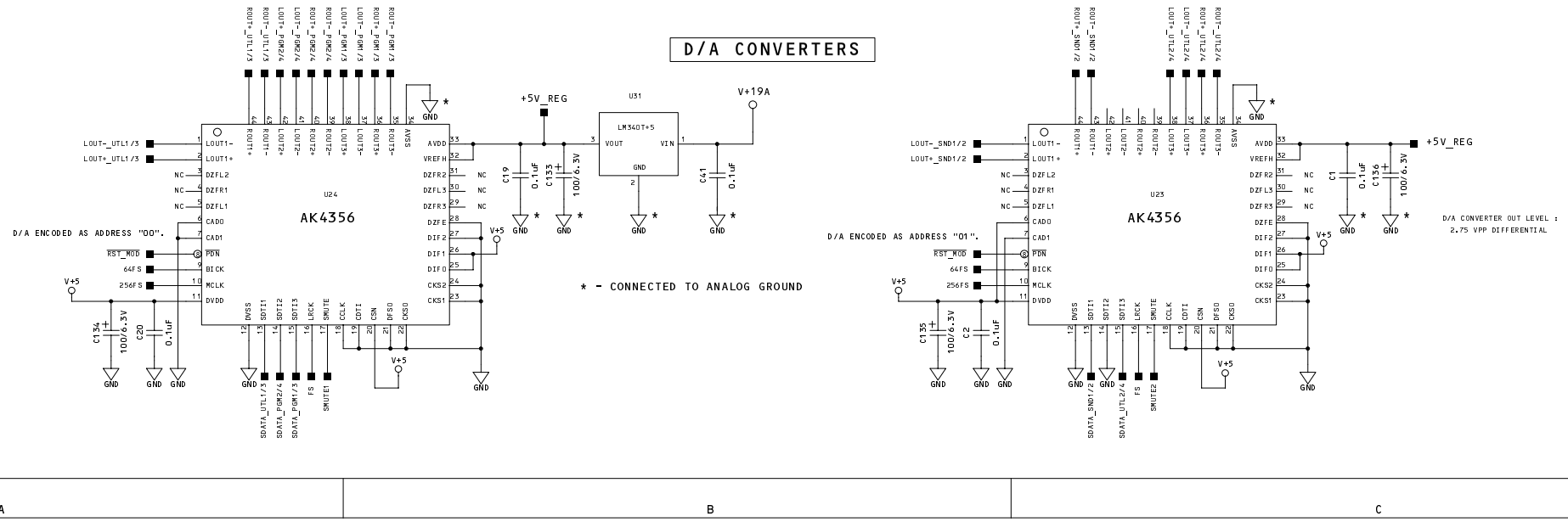
REVISIONS				
REV	ECO #	DESCRIPTION	DATE	APPROVAL
A		INITIAL RELEASE	6/29/01	J. Dombrowski
B	4655	DESIGNS ERRORS	8/21/01	J. Dombrowski
C	4728	ESD PROTECTION	1/18/02	J. Dombrowski

TRIMABLE OUTPUT STAGES



D/A CONVERTERS



APPROVALS	DATE
J DOMBROWKSI	6/29/01

USED ON BMX DIG/LEGACY

HARRIS CORPORATION BROADCAST SYSTEMS DIVISION
DESIGNS BY PACIFIC RESEARCH & ENGINEERING

SCHEMATIC

OUTPUT 2/3 BOARD

SIZE	DRAWING NUMBER	REV
D	92-1156	C

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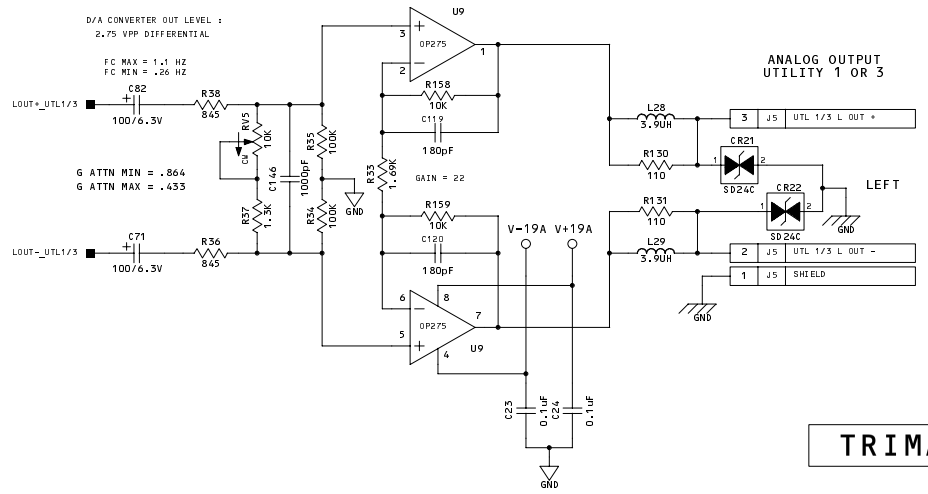
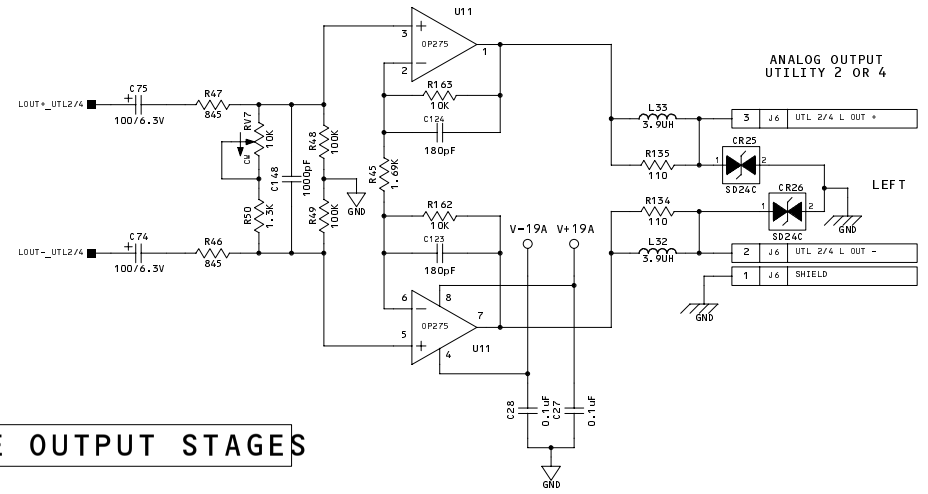
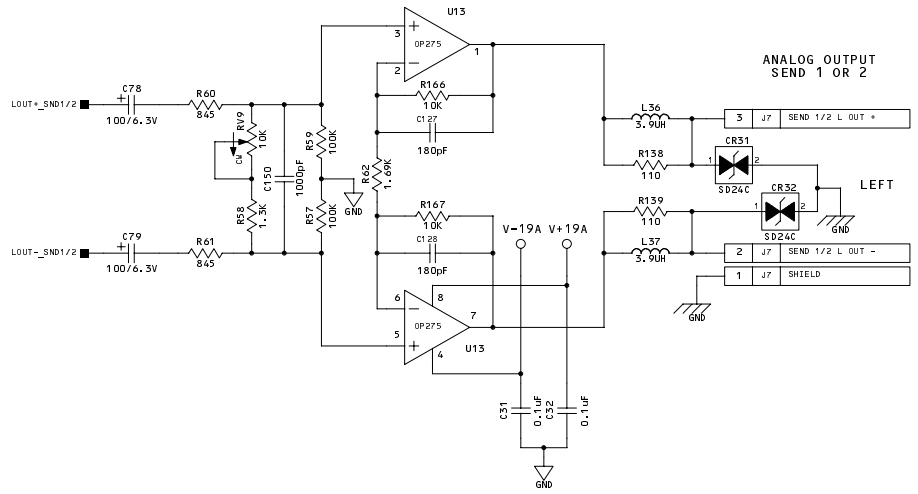
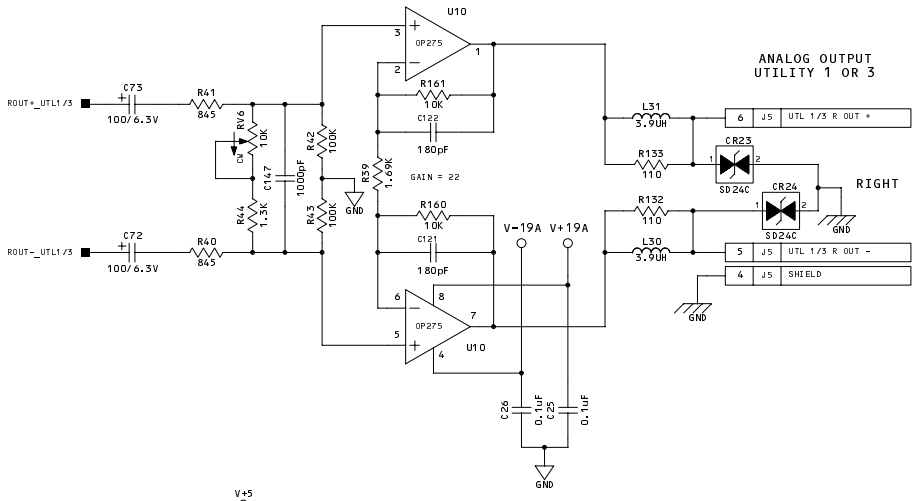
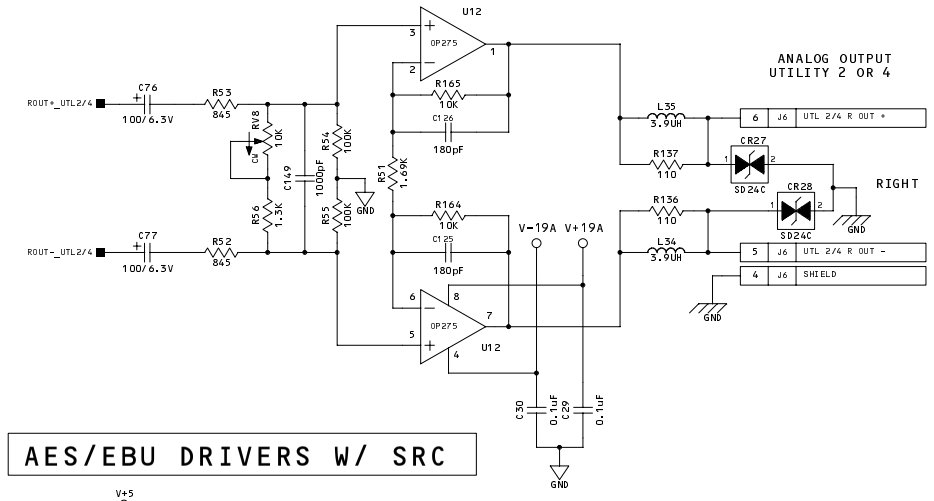


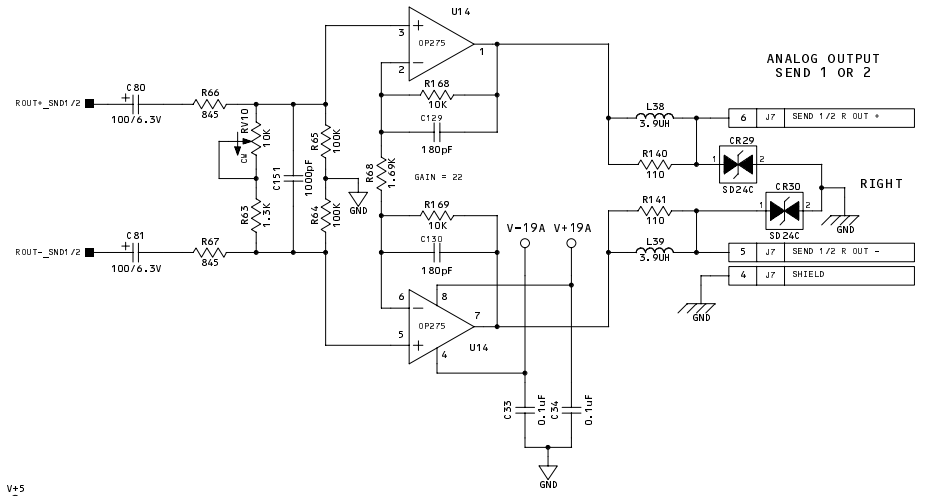




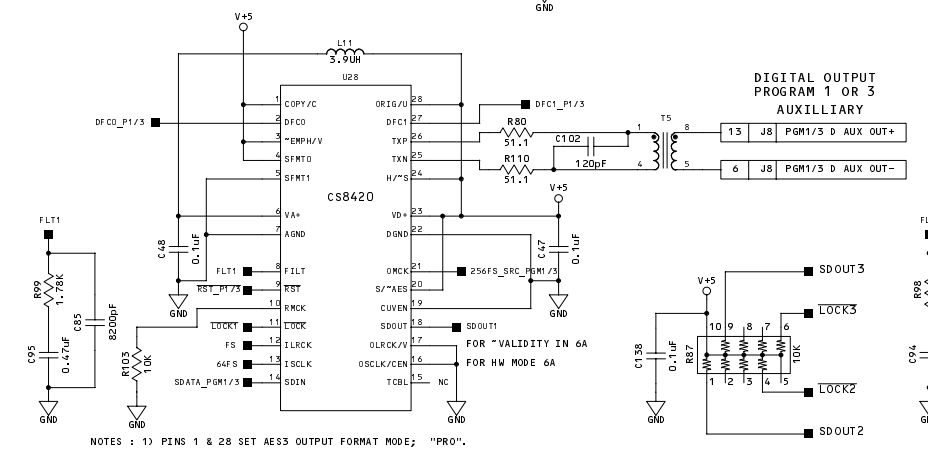
TRIMABLE OUTPUT STAGES

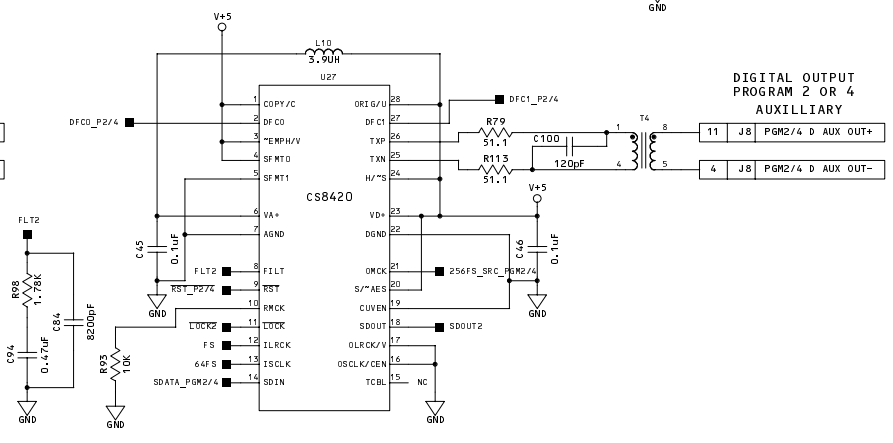


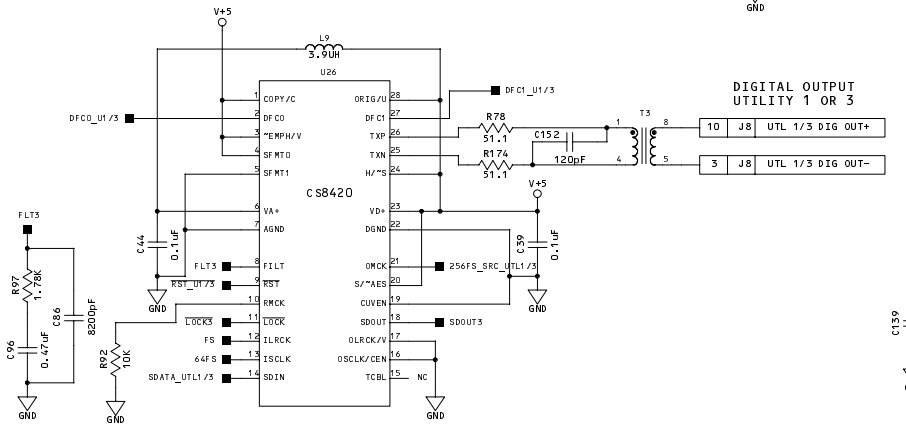




AES/EBU DRIVERS W/ SRC

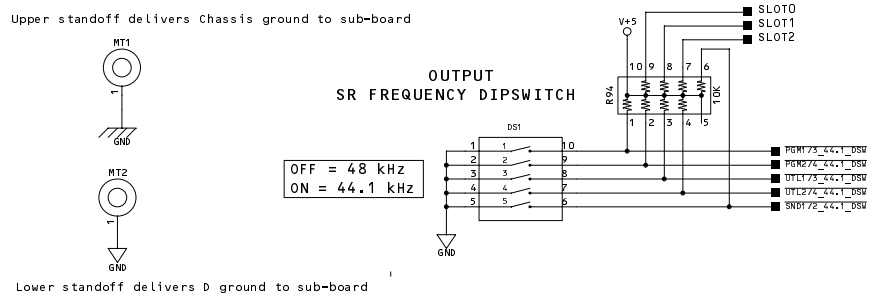




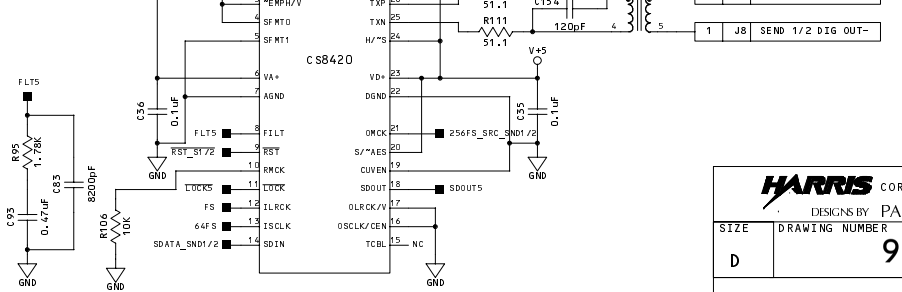


NOTES : 1) PINS 1 & 28 SET AES3 OUTPUT FORMAT MODE; "PRO".
2) PINS 2, 20 & 27 SET UP HARDWARE MODE ; DEFAULT DATA FLOW, SERIAL INPUT, MODE 2.
3) PINS 3 SETS UP EMPHASIS MODE ; NO EMPHASIS.
4) PINS 4 & 5 SET UP SERIAL AUDIO IN/OUT FORMAT MODE ; I2S IN & I2S OUT.
5) PIN 11 (START UP OPTION) SETS UP CH STATUS BLOCK START (PIN 15) AS INPUT/OUTPUT; OUTPUT.
6) PIN 18 (START UP OPTION) SETS UP SERIAL DATA OUT PORT; MASTER.
7) PIN 19 SETS UP MODE 24/28; MODE2A , CH STATUS BITS SET.
8) PIN 20 SELECTS SERIAL AUDIO INPUT SOURCE AES3/SERIAL; SERIAL.
9) PIN 24 SETS UP HARWARE/SOFTWARE MODE; HARDWARE, NO MICRO.

Upper standoff delivers Chassis ground to sub-board



Lower standoff delivers D ground to sub-board



HARRIS CORPORATION BROADCAST SYSTEMS DIVISION
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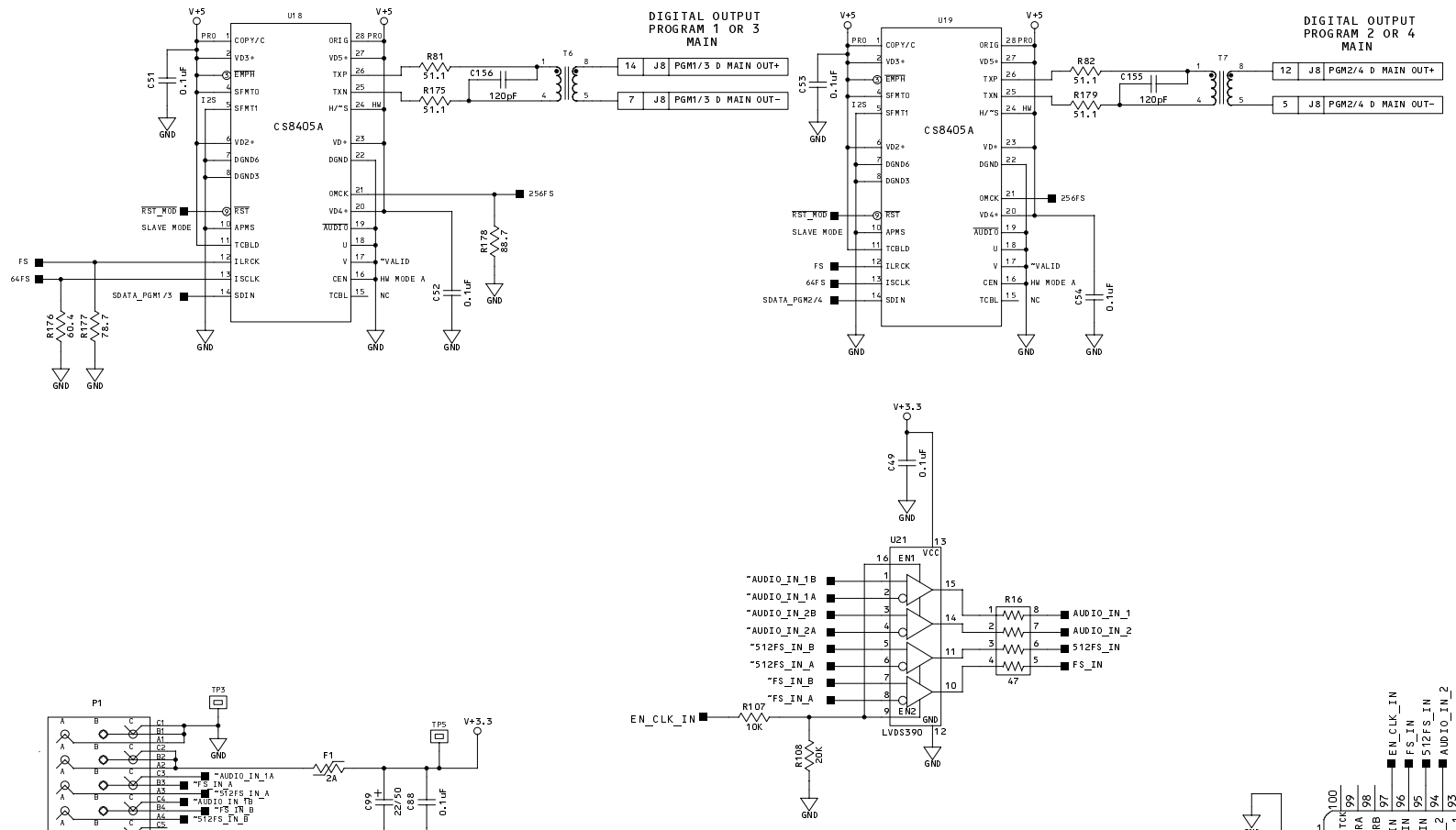
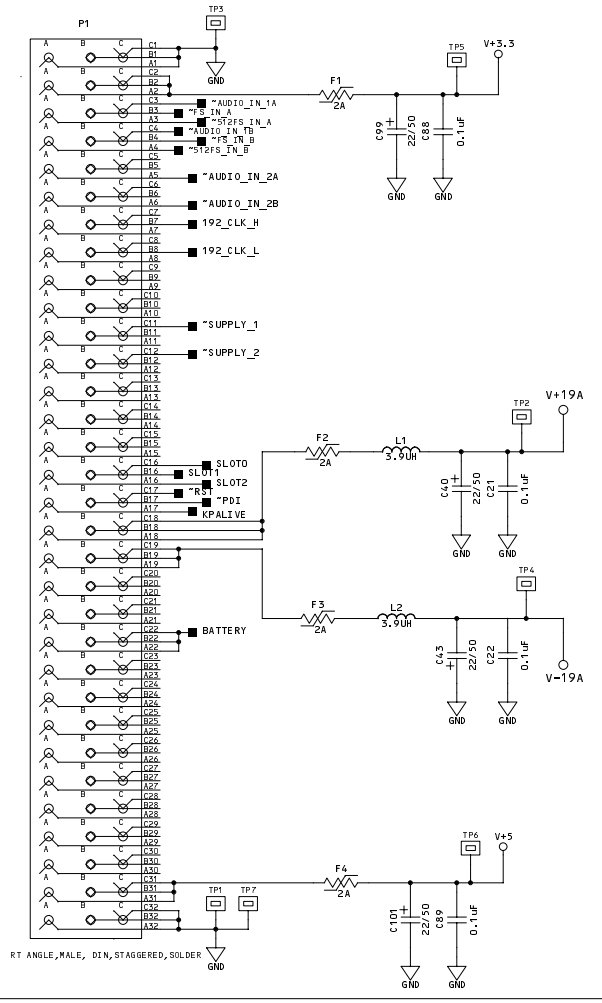
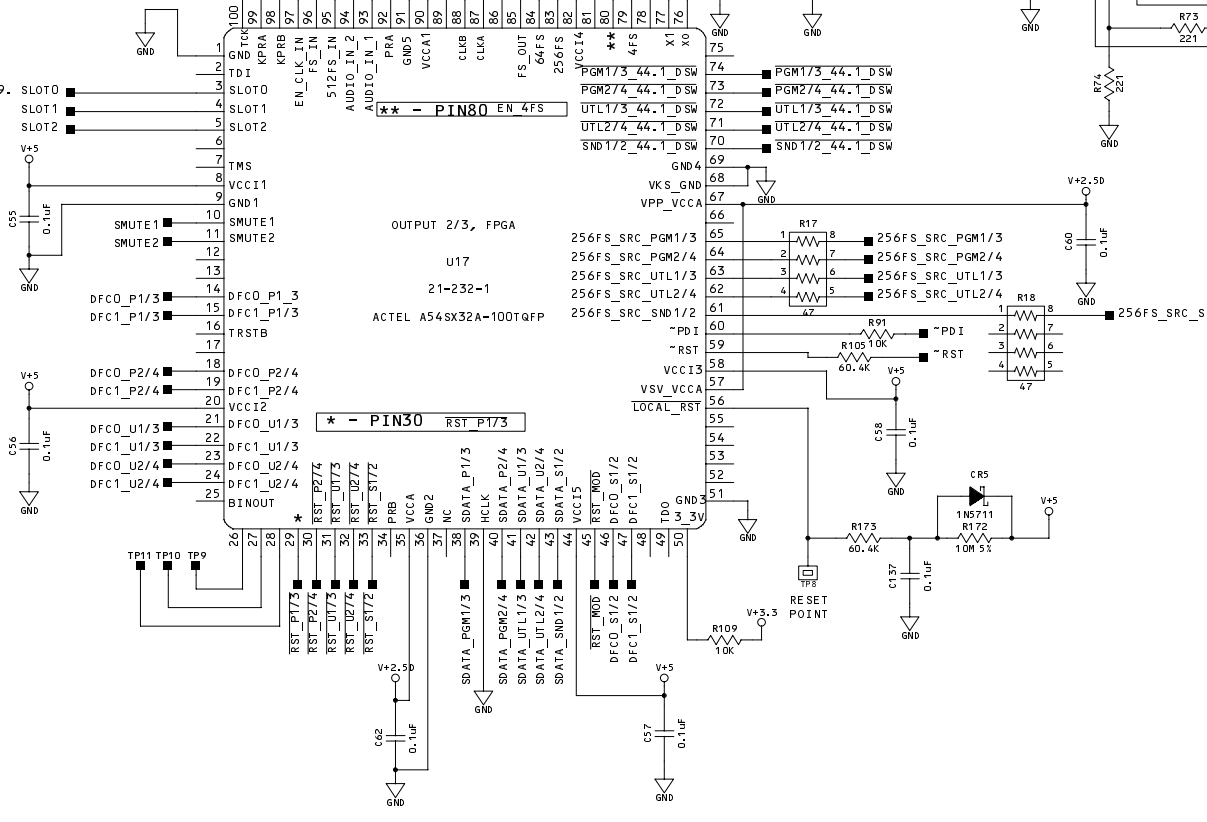
AES/EBU DRIVERS

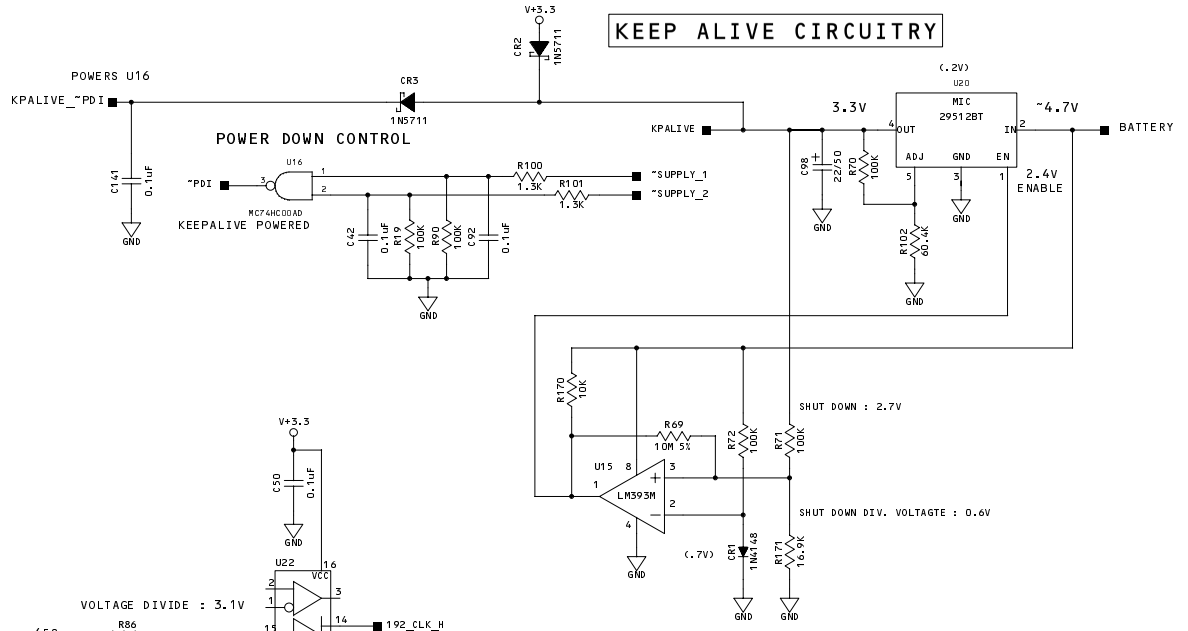




Note : SLOT 0 is pulled by R89.

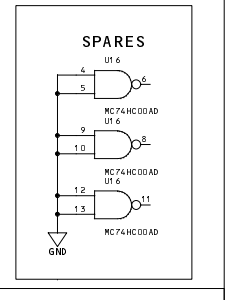


KEEP ALIVE CIRCUITRY



FPGA

SPARES



HARRIS CORPORATION BROADCAST SYSTEMS DIVISION		
DESIGNS BY PACIFIC RESEARCH & ENGINEERING		
SIZE D	DRAWING NUMBER 92-1156	REV C
1-7-2002_9:58	SHEET 3 OF 3	